CLAIMS

What is claimed is:

1. An overlay target comprising:

at least one trench including a series of raised lines.

2. The overlay target of claim 1, wherein said at least one trench comprises a continuous trench defining a geometric shape.

3. The overlay target of claim 1, wherein said at least one trench comprises a plurality of trenches defining said overlay target, each of said plurality of trenches including a series of raised lines.

4. The overlay target of claim 3, wherein said plurality of trenches includes at least one continuous trench defining a geometric shape.

5. An overlay target comprising:

at least one pad area including a series of raised lines.

6. The overlay target of claim 6, wherein said at least one pad area includes a plurality of pad areas defining said overlay target, each of said pad areas including a series of raised lines.

7. The overlay target of claim 6, further comprising at least one trench including a series of raised lines.

8. A semiconductor wafer comprising:

a semiconductor substrate; and

9. The semiconductor wafer of claim 8, wherein said at least one series of raised lines is etched into said semiconductor substrate.

10. The semiconductor wafer of claim 8, wherein said at least one series of raised lines is etched into a material layer overlying said semiconductor substrate.

11. The semiconductor wafer of claim 8, wherein said at least one series of raised lines of is disposed in at least one trench.

12. The semiconductor wafer of claim 11, wherein a plurality of trenches and a corresponding plurality of series of raised lines define said overlay target, each of said plurality of trenches including one of said plurality of series raised lines.

13. The semiconductor wafer of claim 8, wherein said at least one series of raised lines is disposed in at least one pad area.

14. The semiconductor wafer of claim 13, wherein a plurality of pad areas and a corresponding plurality of series of raised lines define said overlay target, each of said plurality of pad areas including one of said plurality of series of raised lines.

15. The semiconductor wafer of claims 8, wherein said at least one series of raised lines comprises a first series of raised lines disposed in a pad area and a second series of raised lines disposed in a trench.

16. A method for forming an overlay target including a series of raised lines, the method comprising:

providing a substrate;

depositing a resist layer over said substrate;

patterning said resist layer to include a pattern defining said overlay target including a series of raised lines; and

etching said substrate to form said overlay target including a series of raised lines.

17. The method of claim 16, wherein providing a substrate comprises providing a semiconductor substrate selected from the group consisting of silicon, gallium, and sapphire substrates.

18. The method of claim 17, wherein depositing a resist layer over said substrate comprises depositing a resist layer directly over said semiconductor substrate selected from the group consisting of silicon, gallium, and sapphire substrates

19. The method of claim 16, wherein providing a substrate includes providing a semiconductor substrate having a top surface, a bottom surface, and a material layer deposited over said top surface.

20. The method of claim 19, wherein depositing a resist layer over said substrate comprises depositing a resist layer over said material layer and said etching said substrate to form said overlay target comprises etching said material layer.